## Sup

## WHAT IS CLAIMED IS:

<b>&gt;</b> 1	1. A processing core that executes a compare instruction, the
2	processing core comprising:
3	a plurality of general-purpose registers comprising a first input operand
4	register, a second input operand register and an output operand register;
5	a register file comprising the plurality of general-purpose registers;
6	comparison logic coupled to the register file, wherein the comparison logic
7	tests for at least two of the following relationships: less than, equal to, greater than and no
8	valid relationship;
9	decode logic which selects the output operand register from the plurality of
10	general-purpose registers; and
11	a store path between the comparison logic and the selected output operand
12	register.
1	2. The processing core that executes the compare instruction as set
2	forth in claim 1, wherein a very long instruction word includes a plurality of compare
3	instructions.
1	The supposition are that accounts the common instruction as set
1	3. The processing core that executes the compare instruction as set
2	forth in claim 1, wherein decode logic selects the first and second input operand registers
3	from the plurality of general-purpose registers.
1	4. The processing core that executes the compare instruction as set
2	forth in claim 1, wherein the processing core issues a plurality of compare instructions at
3	one time.
1	5. The processing core that executes the compare instruction as set
2	forth in claim 1, further comprising:
3	a first load path between the first input operand register and comparison
4	logic; and
5	a second load path between the second input operand register and
6	comparison logic.
1	6. The processing core that executes the compare instruction as set
2	forth in claim 1, wherein the output operator register stores a value indicating a

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relationship between the first and second input operator registers which is at least one of 3 4 greater than, less than, equal to and not a number. 7. The processing core that executes the compare instruction as set 1 forth in claim 6, wherein the not a number value indicates a comparison between the first 2 3 and second input operands that cannot be made. The processing core that executes the compare instruction as set 1 8. 2 forth in claim 6, wherein the value is an integer. The processing dore that executes the compare instruction as set 1 9. 2 forth in claim 1, wherein: the first input operand register is a double precision floating point data 3 4 type; the second input operand register is a single precision floating point data 5 6 type; and the output operand register is a double precision floating point data type. 7 10. The processing core that executes the compare instruction as set 1 forth in claim 1, further comprising a plurality of processing paths that are coupled to the 2 3 register file. 1 11. The processing core that executes the compare instruction as set forth in claim 1, wherein the register file comprises special purpose registers which 2 3 cannot store an output operand. A method for performing a compare operation, the method 1 12. 2 comprising steps of: 3 decoding a compare instruction; configuring first and second paths between a register file and comparison 4

logic; 6

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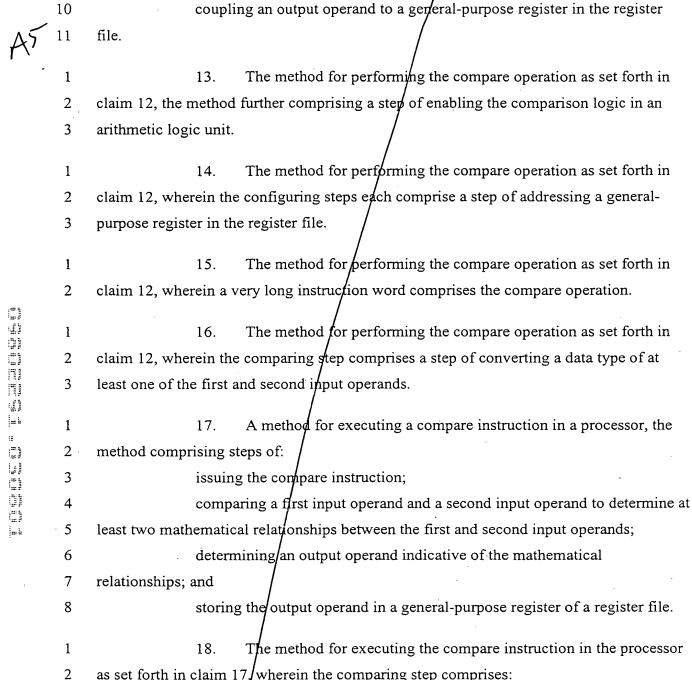
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configuring a third path between the comparison logic and the register file; comparing a first input operand and a second input operand to produce a

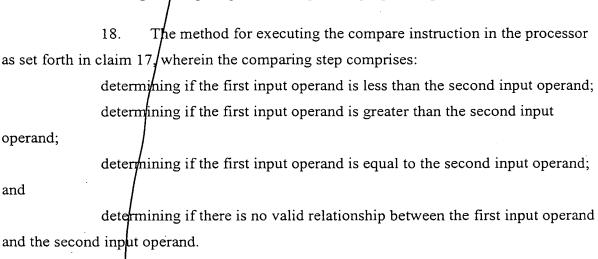
result which indicates an absence of at least three mathematical relationships between the

first input operand and the second input operand; and



operand;

and



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1	19. The method for executing the compare instruction in the processor
2	as set forth in claim 17, wherein the compare instruction is a very long instruction word
3	which comprises a plurality of compare instructions which are processed in parallel down
4 .	separate processing paths.
1	20. The phethod for executing the compare instruction in the processor
2	as set forth in claim 17, wherein the general-purpose register is used to store operators

3 from other types of instructions.